



SBOS161A – JANUARY 1989 – REVISED JULY 2003

Precision Dual *Difet*® Operational Amplifier

FEATURES

- Very Low Noise: $8\text{nV}/\sqrt{\text{Hz}}$ at 10kHz
- Low V_{OS} : 1mV max
- Low Drift: $10\mu\text{V}/^\circ\text{C}$ max
- Low I_B : 10pA max
- Fast Settling Time: 2 μs to 0.01%
- Unity-Gain Stable

APPLICATIONS

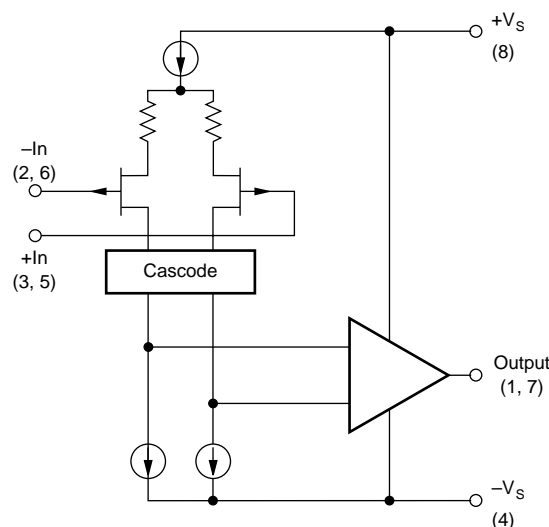
- Data Acquisition
- DAC Output Amplifiers
- Optoelectronics
- High-Impedance Sensor Amps
- High-Performance Audio Circuitry
- Medical Equipment, CT Scanners

DESCRIPTION

The OPA2107 dual operational amplifier provides precision *Difet* performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET® type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (*Difet*) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent dc performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in DIP-8 and SO-8 packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	±18V
Input Voltage Range	±V _S ±2V
Differential Input Voltage	Total V _S ±4V
Operating Temperature	
P and U Packages	–25°C to +85°C
Storage Temperature	
P and U Packages	–40°C to +125°C
Output Short Circuit to Ground (T _A = +25°C)	Continuous
Junction Temperature	+175°C
Lead Temperature	
P Package (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C

NOTE: Stresses above these ratings may cause permanent damage.



ELECTROSTATIC DISCHARGE SENSITIVITY

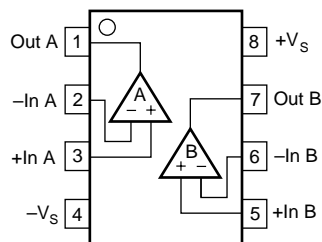
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View

DIP, SO



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2107	DIP-8	P	–25°C to +85°C	OPA2107AP	OPA2107AP	Tube, 50
OPA2107	SO-8	D	–25°C to +85°C	OPA2107AU	OPA2107AU	Tube, 100
"	"	"	"	"	OPA2107AU/2K5	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

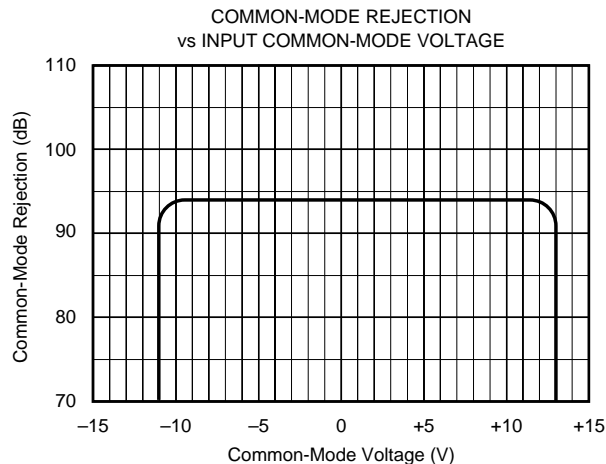
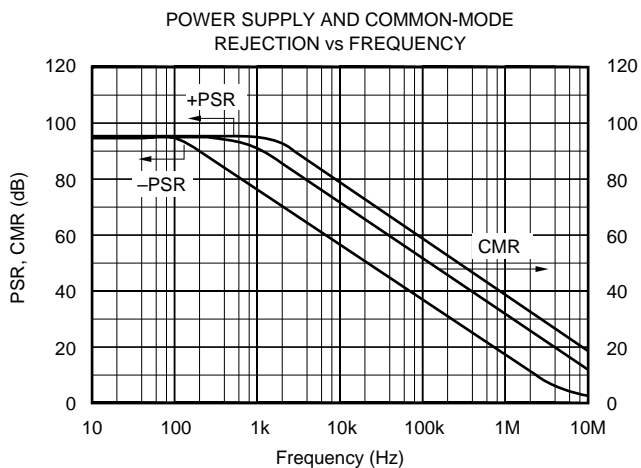
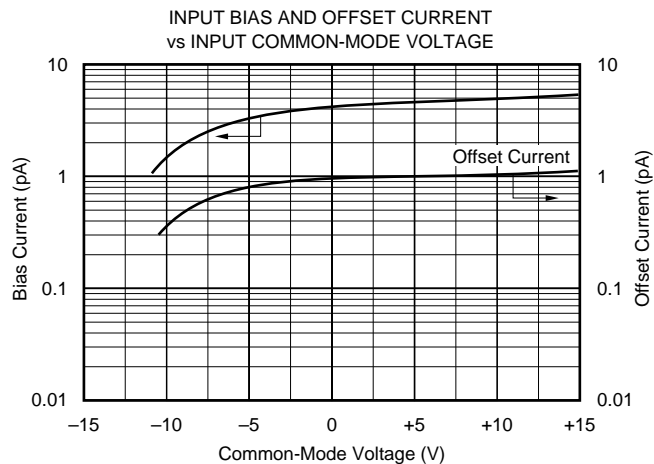
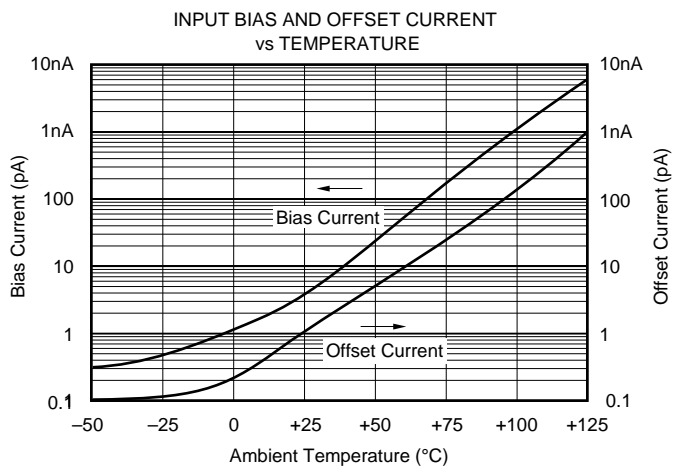
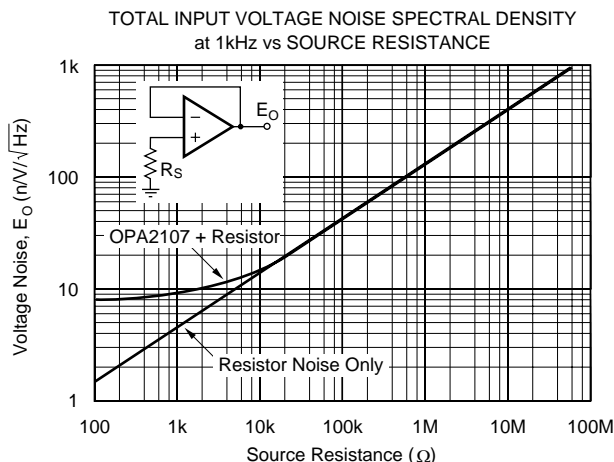
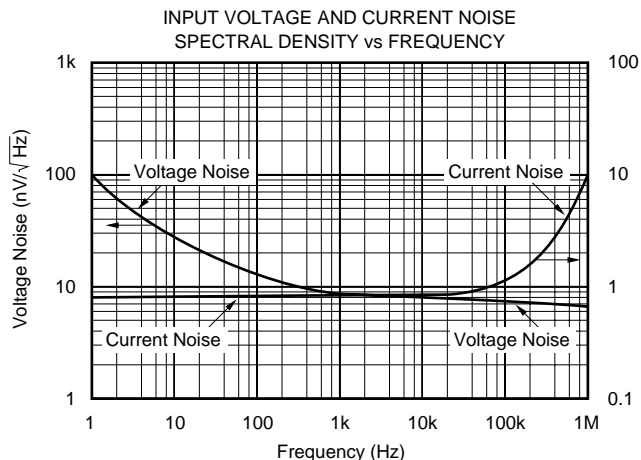
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

PARAMETER	CONDITION	OPA2107AP, AU			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Over Specified Temperature Average Drift Over Specified Temperature Power Supply Rejection	$V_{CM} = 0\text{V}$ $V_S = \pm 10 \text{ to } \pm 18\text{V}$	 80	0.1 0.5 3 96	1 2 10	mV mV $\mu\text{V}/^\circ\text{C}$ dB
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Over Specified Temperature Input Offset Current Over Specified Temperature	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		4 0.25 1	10 1.5 8 1	pA nA pA nA
INPUT NOISE Voltage: $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ $\text{BW} = 0.1 \text{ to } 10\text{Hz}$ $\text{BW} = 10 \text{ to } 10\text{kHz}$ Current: $f = 0.1\text{Hz}$ thru 20kHz $\text{BW} = 0.1\text{Hz}$ to 10Hz	$R_S = 0$		30 12 9 8 1.2 0.85 1.2 23		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$ μVrms $\text{fA}/\sqrt{\text{Hz}}$ fAp-p
INPUT IMPEDANCE Differential Common-Mode			$10^{13} \parallel 2$ $10^{14} \parallel 4$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
INPUT VOLTAGE RANGE Common-Mode Input Range Over Specified Temperature Common-Mode Rejection	$V_{CM} = \pm 10\text{V}$	± 10.5 ± 10.2 80	± 11 ± 10.5 94		V V dB
OPEN-LOOP GAIN Open-Loop Voltage Gain Over Specified Temperature	$V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	82 80	96 94		dB dB
DYNAMIC RESPONSE Slew Rate Settling Time: 0.1% 0.01% Gain Bandwidth Product THD + Noise Channel Separation	$G = +1$ $G = -1$, 10V Step $G = 100$ $G = +1$, $f = 1\text{kHz}$ $f = 100\text{Hz}$, $R_L = 2\text{k}\Omega$	13	18 1.5 2 4.5 0.001 120		V/ μs μs μs MHz % dB
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current		± 4.5	± 15 ± 4.5		V V mA
OUTPUT Voltage Output Over Specified Temperature Short Circuit Current Output Resistance, Open-Loop Capacitive Load Stability	$R_L = 2\text{k}\Omega$ 1MHz $G = +1$	± 11 ± 10.5 ± 10	± 12 ± 11.5 ± 40 70 1000		V V mA Ω pF
TEMPERATURE RANGE Specification Operating Storage Thermal Resistance (θ_{JA}) DIP-8 SO-8		-25 -25 -40		+85 +85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

NOTE: (1) Specified with devices fully warmed up.

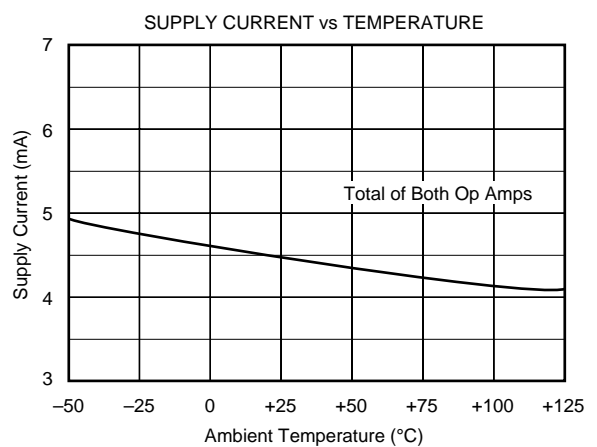
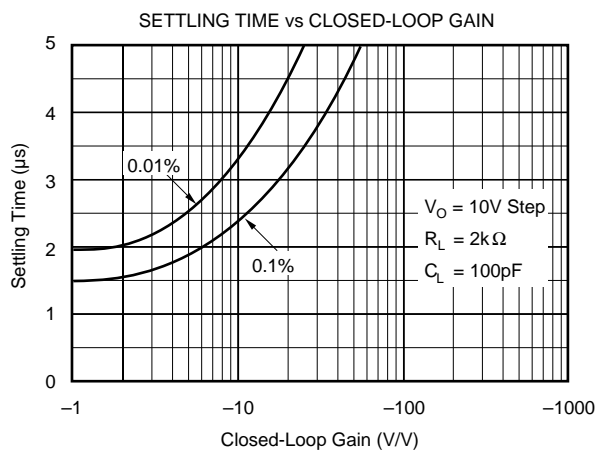
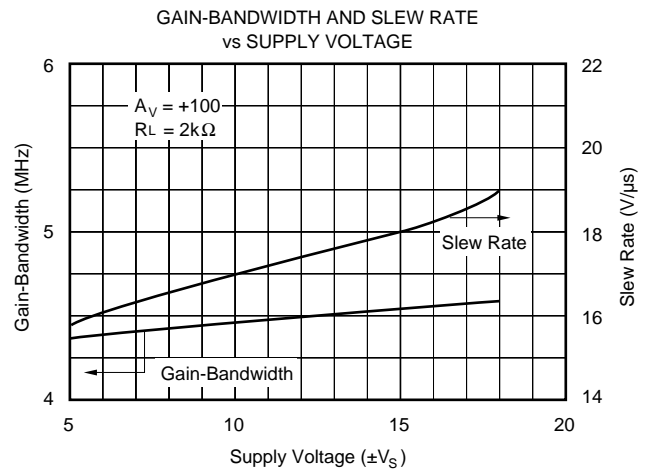
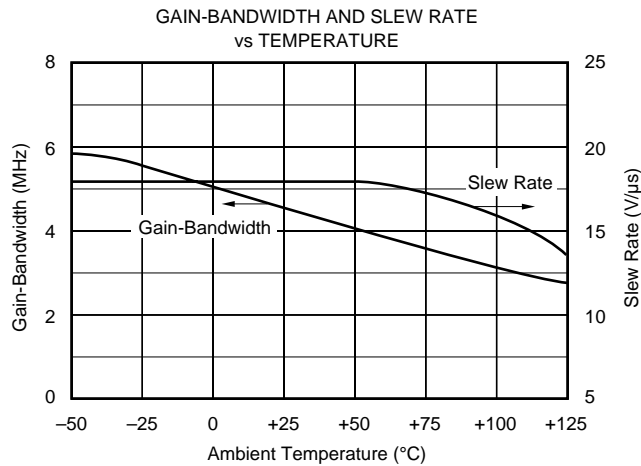
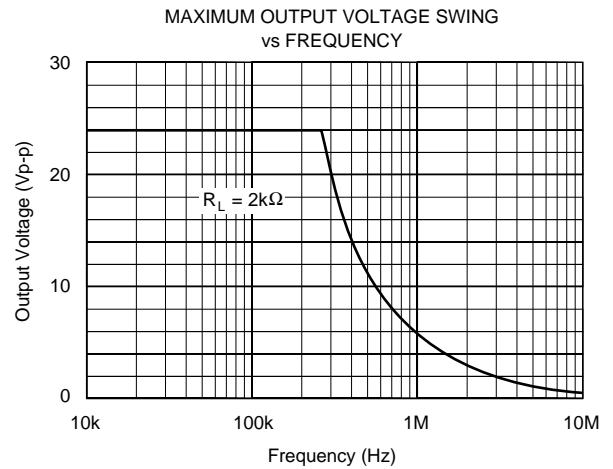
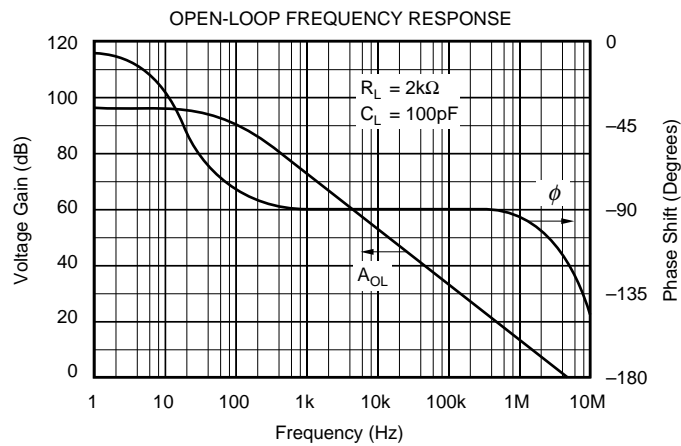
TYPICAL CHARACTERISTICS

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



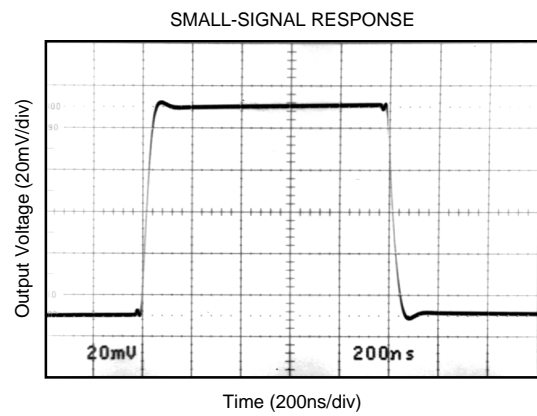
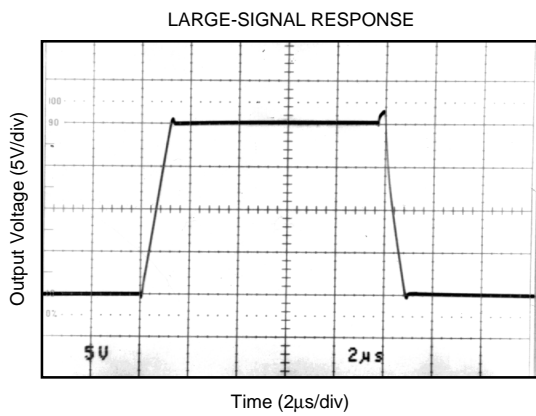
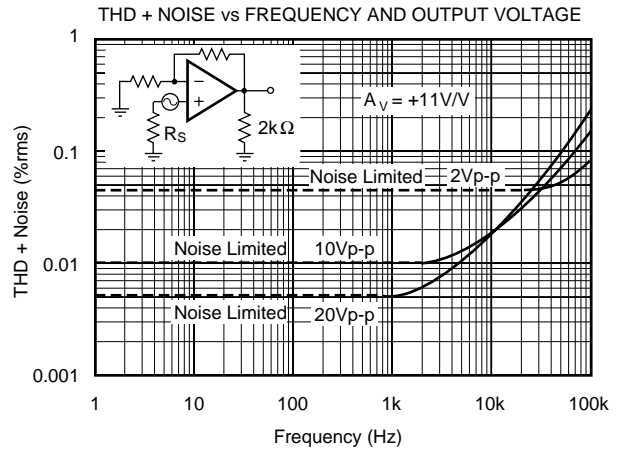
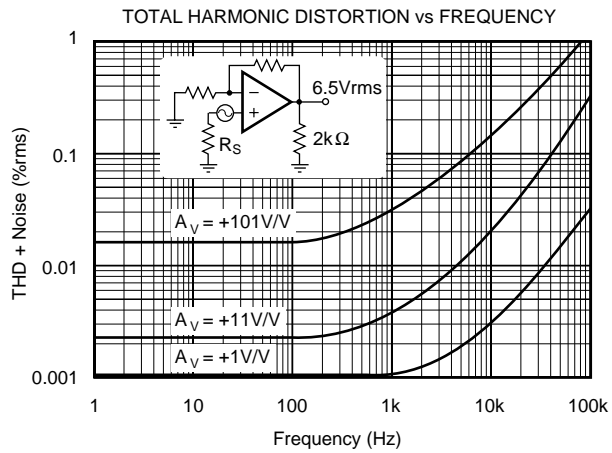
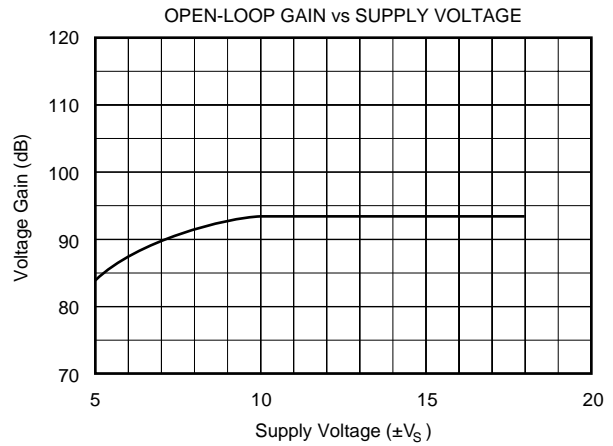
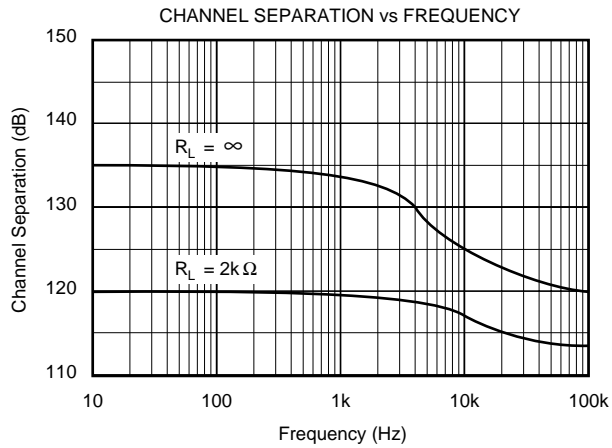
TYPICAL CHARACTERISTICS (Cont.)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION AND CIRCUITS

The OPA2107 is unity-gain stable and has an excellent phase margin. This makes it easy to use in a wide variety of applications.

Power-supply connections should be bypassed with capacitors positioned close to the amplifier pins. In most cases, 0.1µF ceramic capacitors are adequate. Applications with larger load currents and fast transient signals may need up to 1µF tantalum bypass capacitors.

INPUT BIAS CURRENT

The OPA2107 *Difet* input stages have very low input bias current—an order of magnitude lower than BIFET op amps. Circuit-board leakage paths can significantly degrade performance. This is especially evident with the SO-8 surface-mount package where pin-to-pin dimensions are particularly small. Residual soldering flux, dirt, and oils, which conduct leakage current, can be removed by proper cleaning. In most instances, a two-step cleaning process is adequate using a clean organic solvent rinse followed by deionized water. Each rinse should be followed by a 30-minute bake at 85°C. A circuit-board guard pattern effectively reduces errors due to circuit-board leakage (Figure 1). By encircling critical high-impedance nodes with a low-impedance connection at the same circuit potential, any leakage currents will flow harmlessly to the low-impedance node. Guard traces should be placed on all levels of a multiple-layer circuit board.

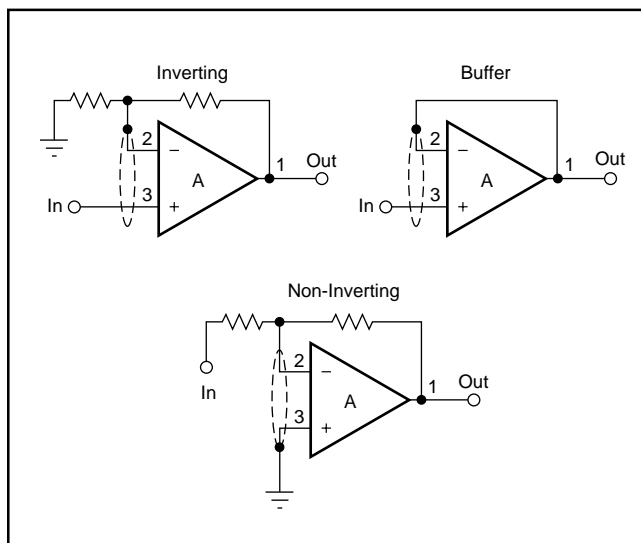


FIGURE 1. Connection of Input Guard.

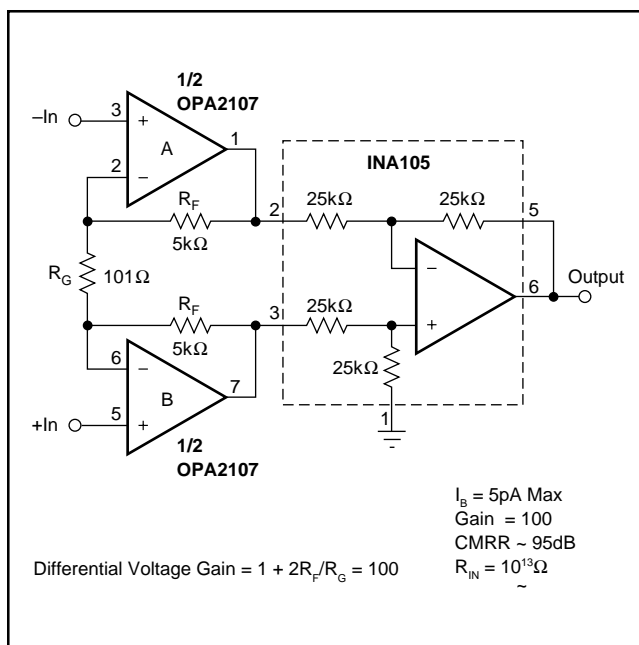


FIGURE 2. FET Input Instrumentation Amplifier.

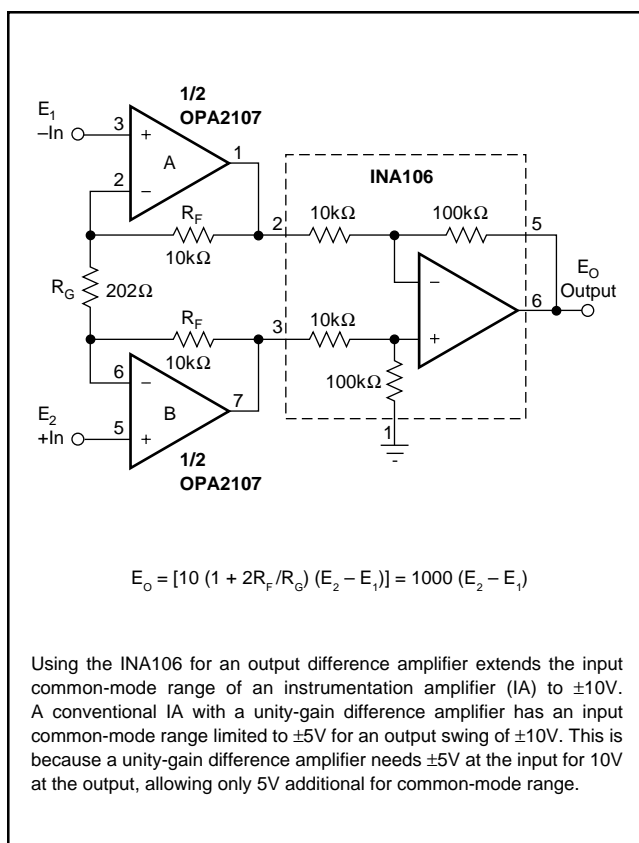


FIGURE 3. Precision Instrumentation Amplifier.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2107AU	NRND	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 80	OPA 2107AU
OPA2107AU.A	NRND	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 2107AU
OPA2107AU/2K5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 2107AU
OPA2107AU/2K5.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 2107AU

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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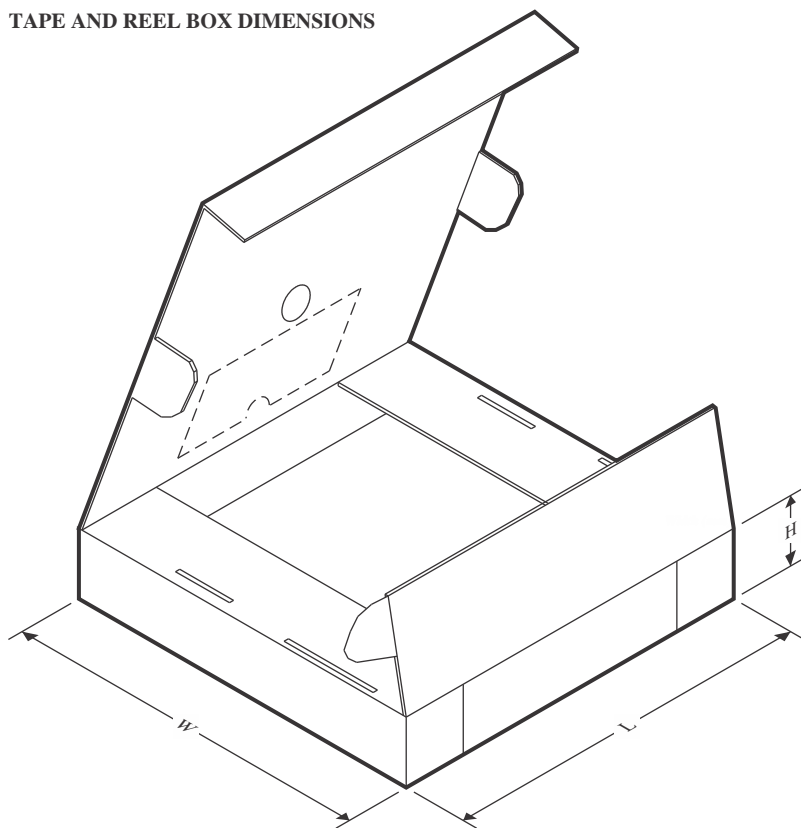
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2107AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

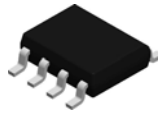
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2107AU/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA2107AU	D	SOIC	8	75	506.6	8	3940	4.32
OPA2107AU.A	D	SOIC	8	75	506.6	8	3940	4.32

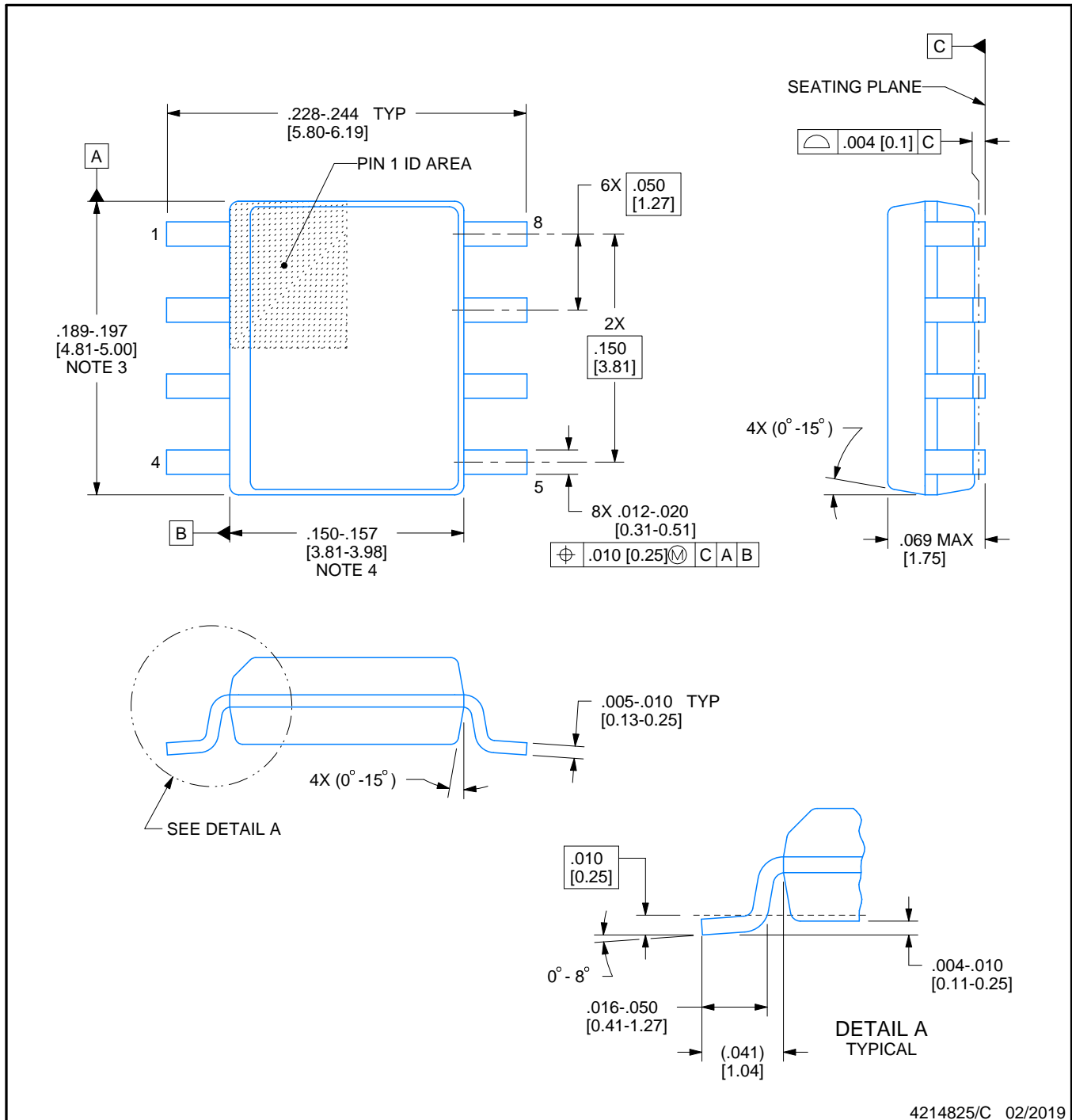


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

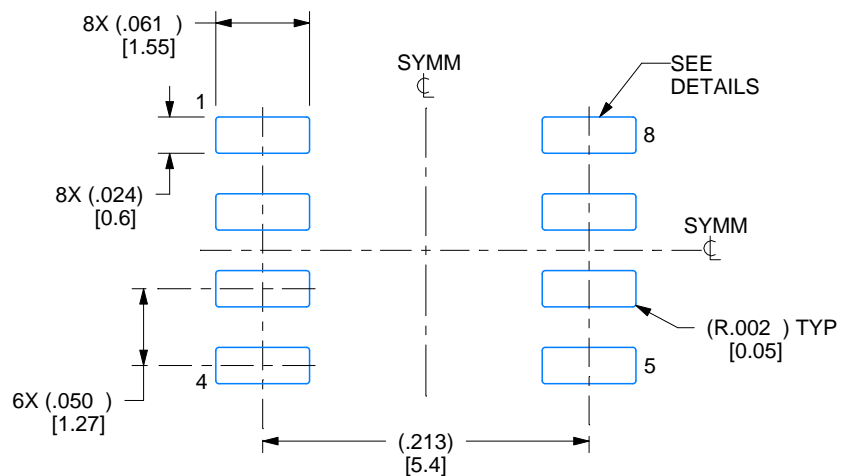
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

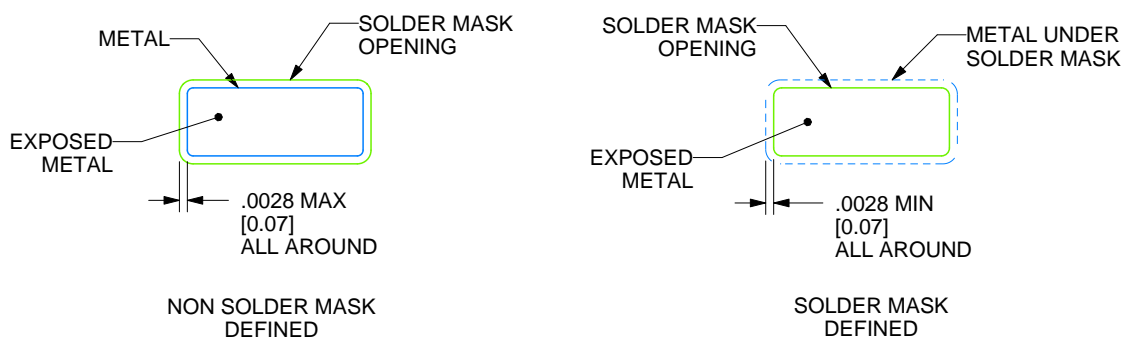
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

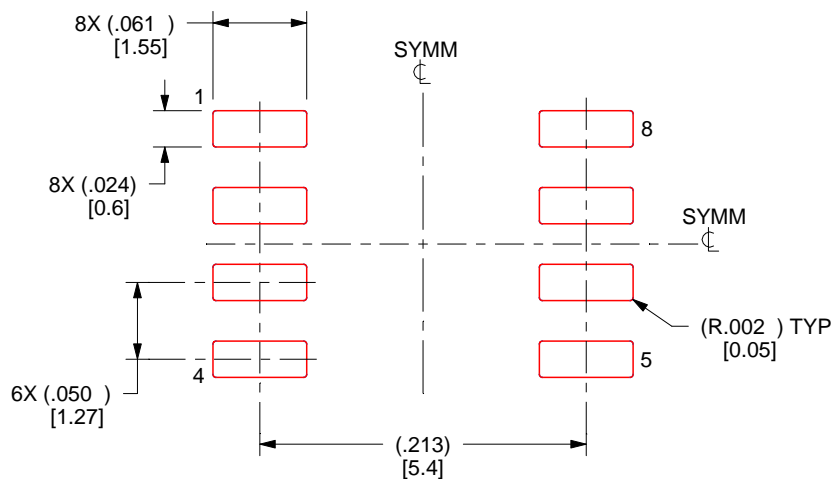
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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